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Detector Characterisation work at Oxford

Dan Weatherill, Ian Shipsey, Lance Miller
& OPMD lab colleagues

Oxford Physics Microstructure Detector Laboratory

Outline

- Introduction
- LSST CCDs background
- Brighter-Fatter Effect Primer
- Selections of work
  - Full well TCAD modelling (phase A & B)
  - Operating point optimisation (phase A & B)
  - CDS timing optimisation (phase A)
  - Single electron trap mapping (phase A & B)
  - Brighter-fatter effect vs gate width (phase B)

A whistle stop tour through some of the things we've been investigating to do with LSST sensor performance

Disclaimers

1) Other than briefly describing it, I will not go into our efforts on modelling brighter-fatter effect (plenty of other talks around about that)

2) I am not going to fully talk about Ian & Lance's phase B PSF modelling proposal (talk to me after if interested)

3) I'm attempting to provide an insight into the breadth of work we're doing for the camera, but very lacking depth – please ask me offline for the gory details!)

OPMD Lab

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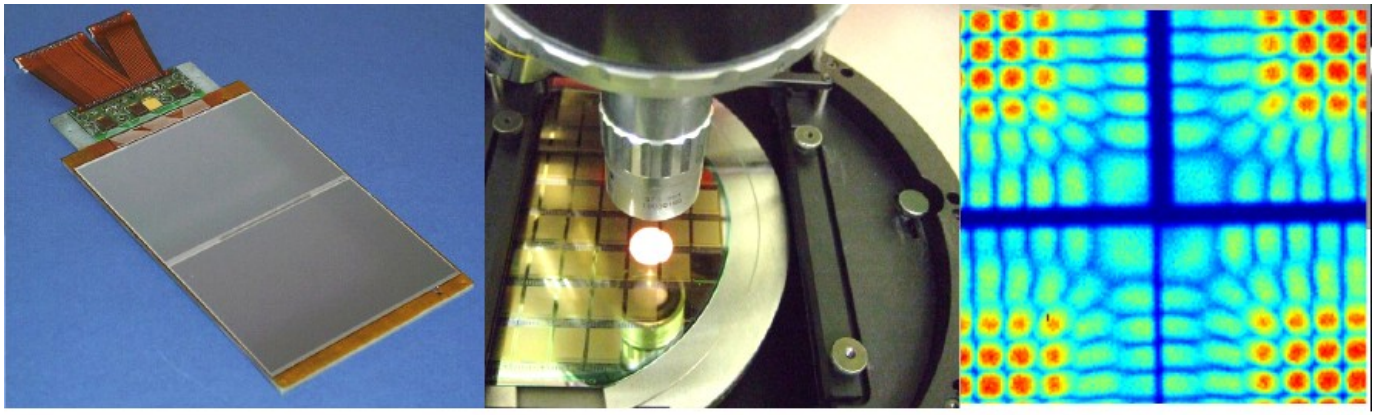

Oxford Physics Microstructure Detector (OPMD) Lab

Silicon Detector Development for:

- Particle Physics (e.g. ATLAS, Mu3e, ATRAP)
- Astrophysics (LSST)
- Photon Science (Medipix / Timepix)

Heads:

Prof I. Shipsey, Prof D. Bortoletto

- 160m^2 ISO 7 cleanroom incorporating a smaller ISO 5 area
- Assembly, wire-bonding, test & measurement facilities

LSST Test System

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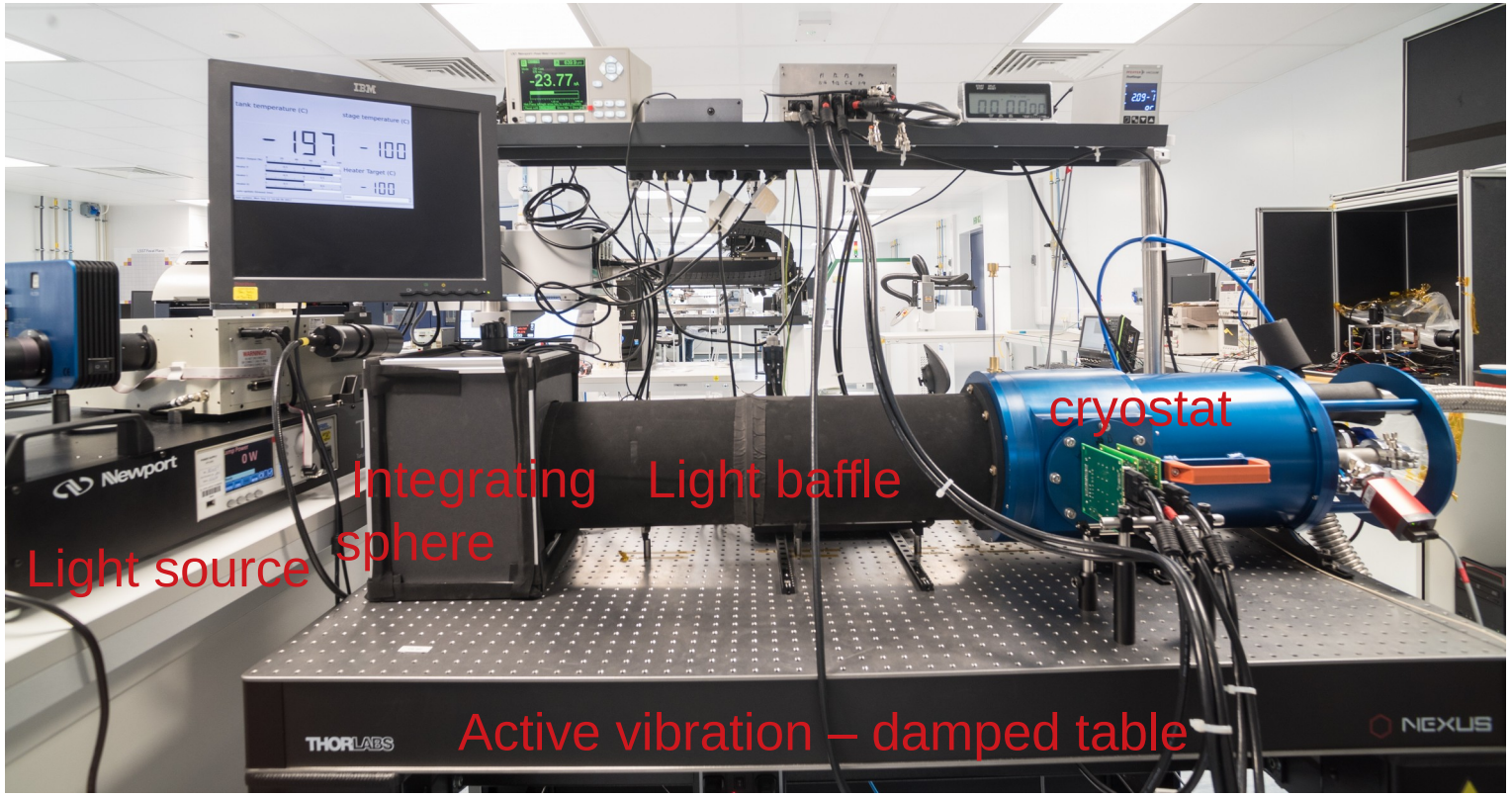
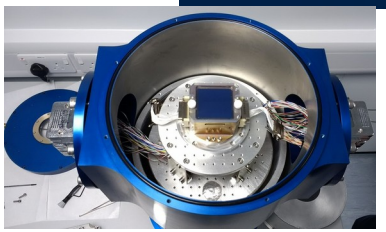
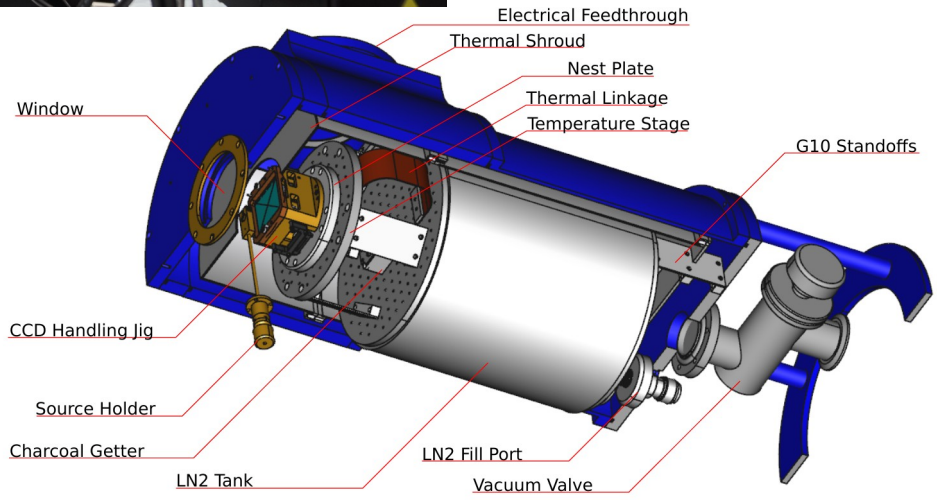




- LN2 cooling and active table for low vibration
- 250W QTH light source + monochromator (300nm – 1600nm wavelength)
- Online radiometry and spectrosopy (at integrating sphere)
- Can quickly swap integrating sphere with projection optics for PSF etc measurements.
- Operates at high vacuum (1E-6 mbar)
- For long periods of time (~weeks per measurement)



LSST sensor requirements

Wide field & Deep – 20000 square degrees, 28th magnitude

Low noise (~5e-)
Back thinned, high QE
10 μm pixels
150 ke- full well capacity
4 side buttable

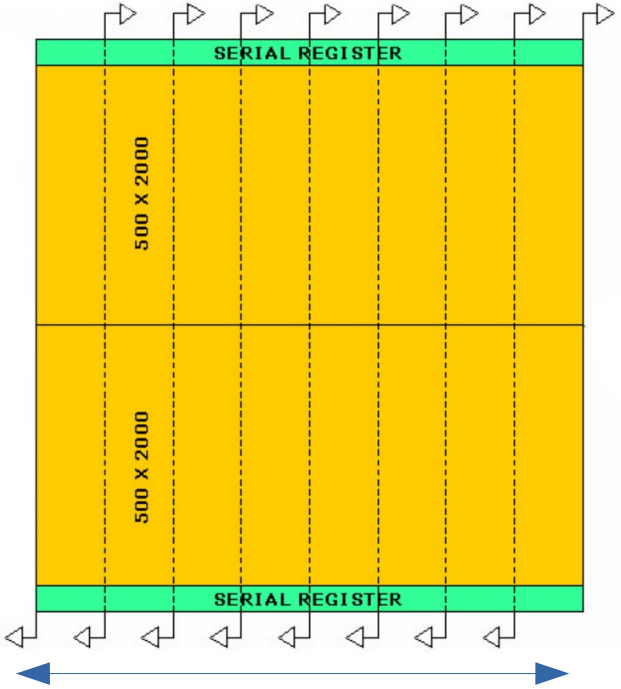


Image: LSST Science Book

So far, standard state of the art scientific CCD
BUT:
Cadence ~ 1minute, readout time 2s

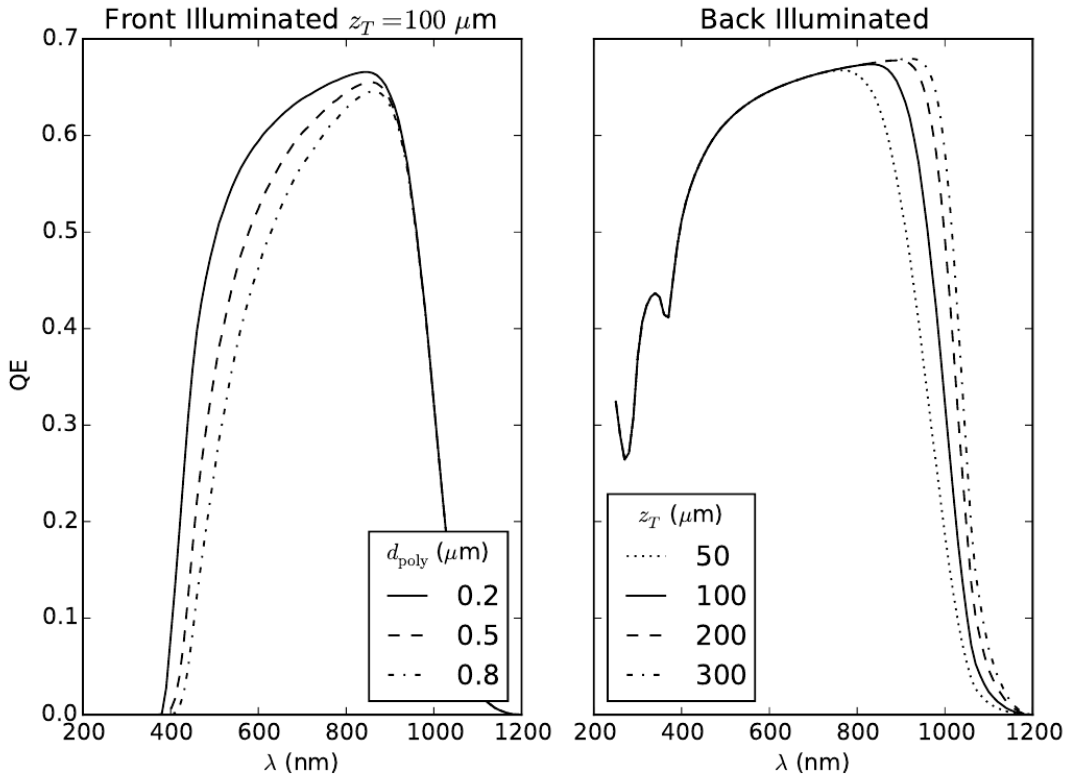
Highly segmented (16 outputs)
"Fast" pixel rate (550kHz)
Extreme sensitivity (reach required depth in 15s exposure)

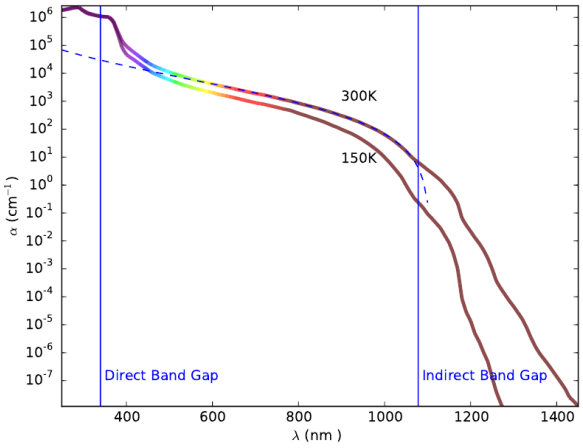
Thick CCDs – What and Why?

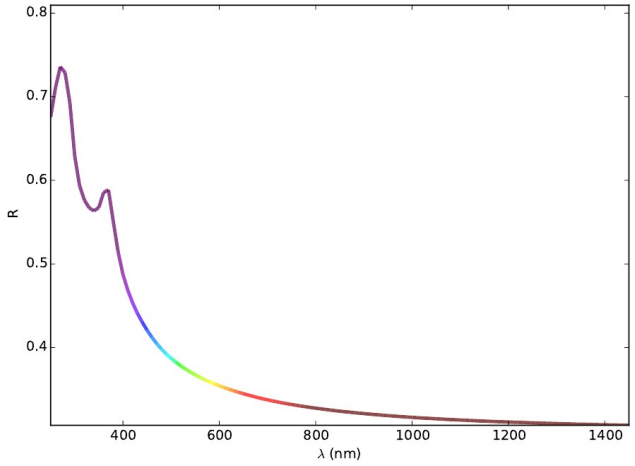
In the context of CCDs, “thick” usually refers to a sensor with active thickness >30μm
Almost always built back-illuminated
Primary advantage – high QE in both the blue (back illumination) and red (thick)
Anti-reflection (AR) coating is of extreme importance to try and “smooth out” the blue QE
(graphs here show uncoated theoretical values)

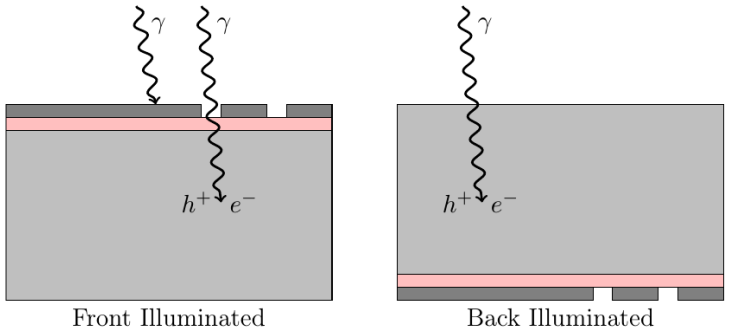
$$QE_{FI} = (1 - R(\lambda))\, e^{-\alpha(\lambda) d_{\mathrm{poly}}} \left(1 - e^{-\alpha(\lambda) z_T}\right)$$

$$QE_{BI} = (1 - R(\lambda)) \left(1 - e^{-\alpha(\lambda) z_T}\right)$$

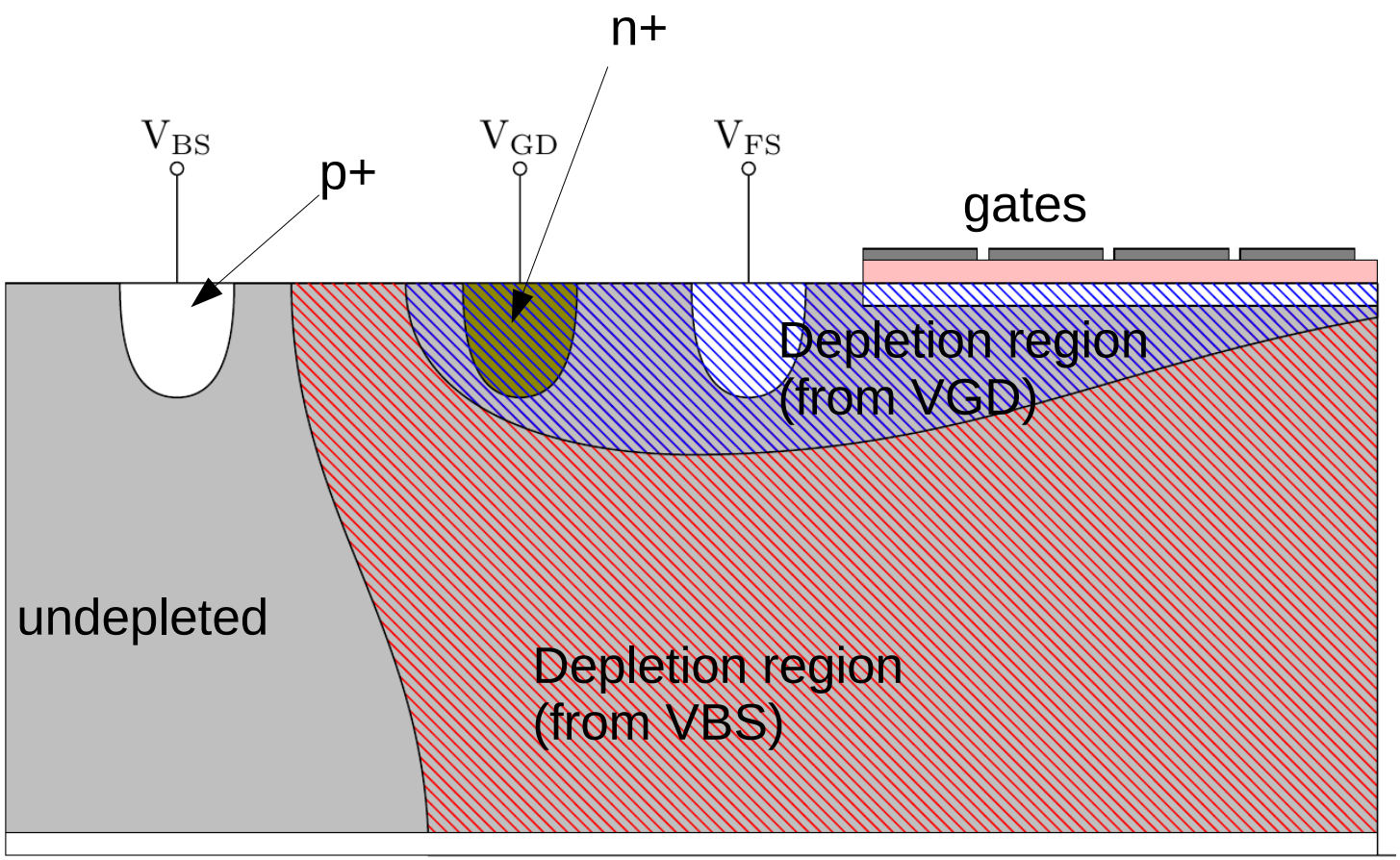








Thick CCDs – how?



A thick detector implies a long drift time for electron collection. This, in turn, implies a large diffusion radius

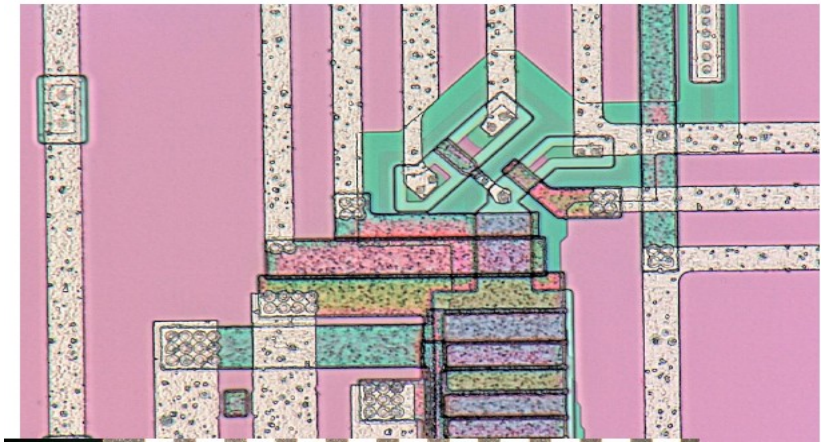
$$r_{\mathrm{diff}} = z_T \sqrt{\frac{2k_B T}{q_e V_{\mathrm{coll}}}}$$

- To reduce the collection time of charges (and thus the diffusion radius), a high bias voltage is applied to the back side of the chip
- In order to prevent leakage currents from the front substrate to the back, guard drains are included in the design which creates a protective depletion region whilst the back bias is applied
- This only works (well) on **fairly exotic high resisitivity bulk silicon**

A Tale of Two Teledyne CCDs

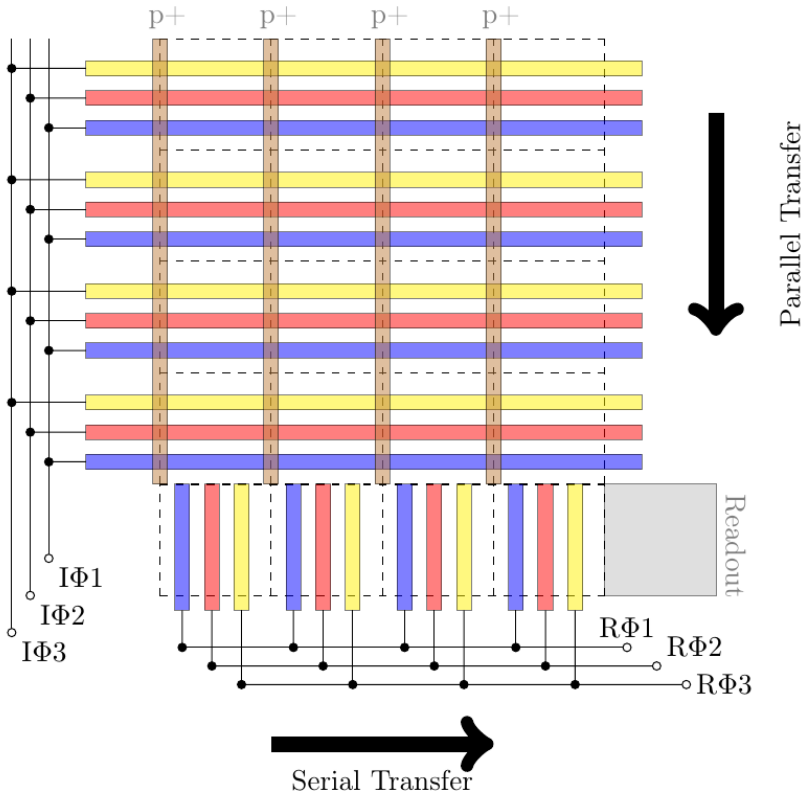
The LSST focal plane contains 189 CCDs, arranged into 21 science rafts. The devices are a mixture of e2v CCD-250 and ITL/STA-3800C. Both are thick, back illuminated CCDs on high resistivity silicon.
But within that constraint, they almost couldn't be more different!

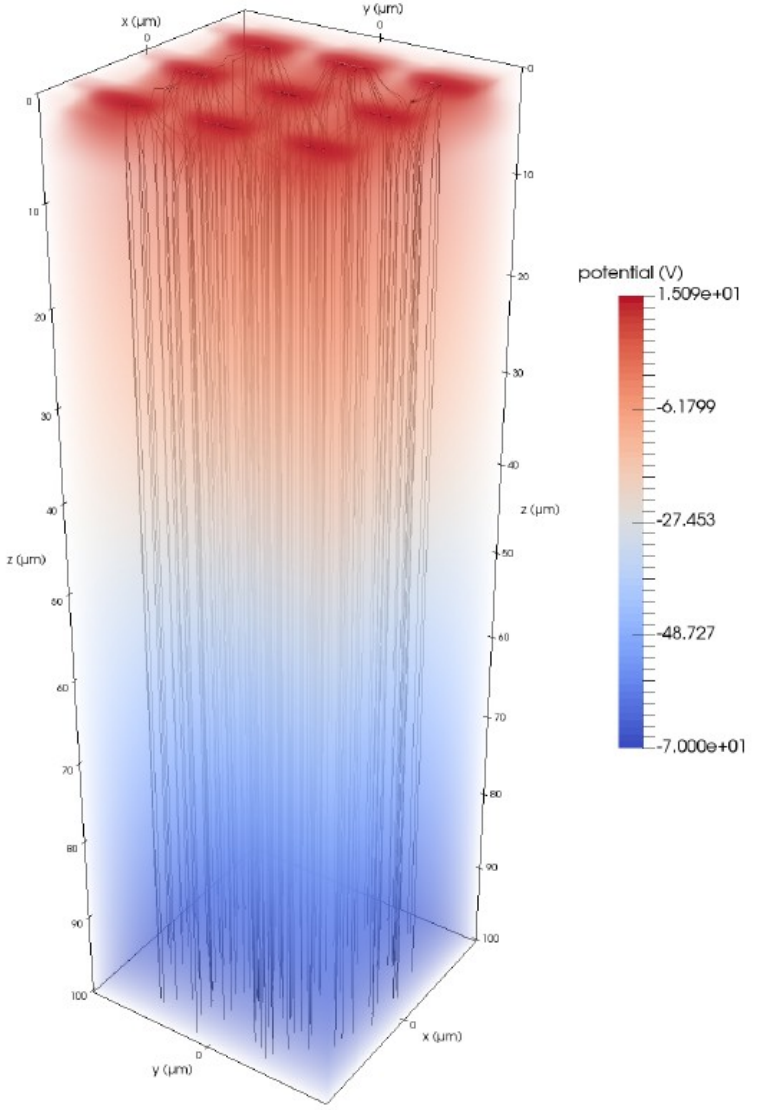
	CCD-250	STA-3800C
Imaging phases	4 (symmetric)	3 (asymmetric)
Output amp	2 stage MOSFET	1 stage JFET
construction	Back thinned, Si substrate	Glued glass substrate with lithoblack coating
Design docs	Very very secret	Available to LSST
Measured performance	Good noise, CTI, linearity	High FWC, better dark current



Measured difference in PSF and brighter-fatter effect sizes between e2v & ITL

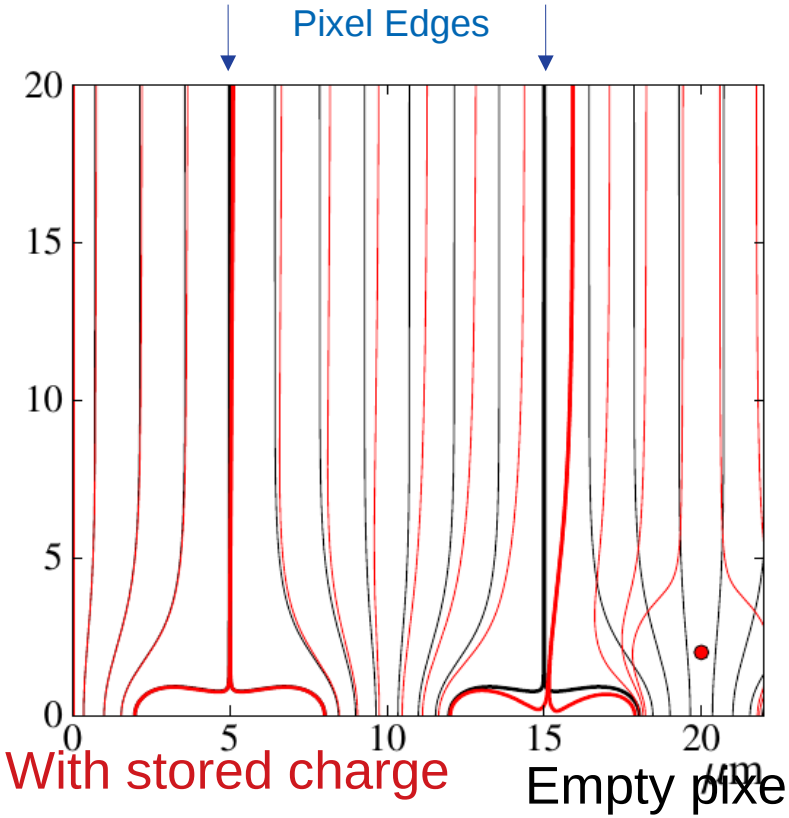
CCD architecture



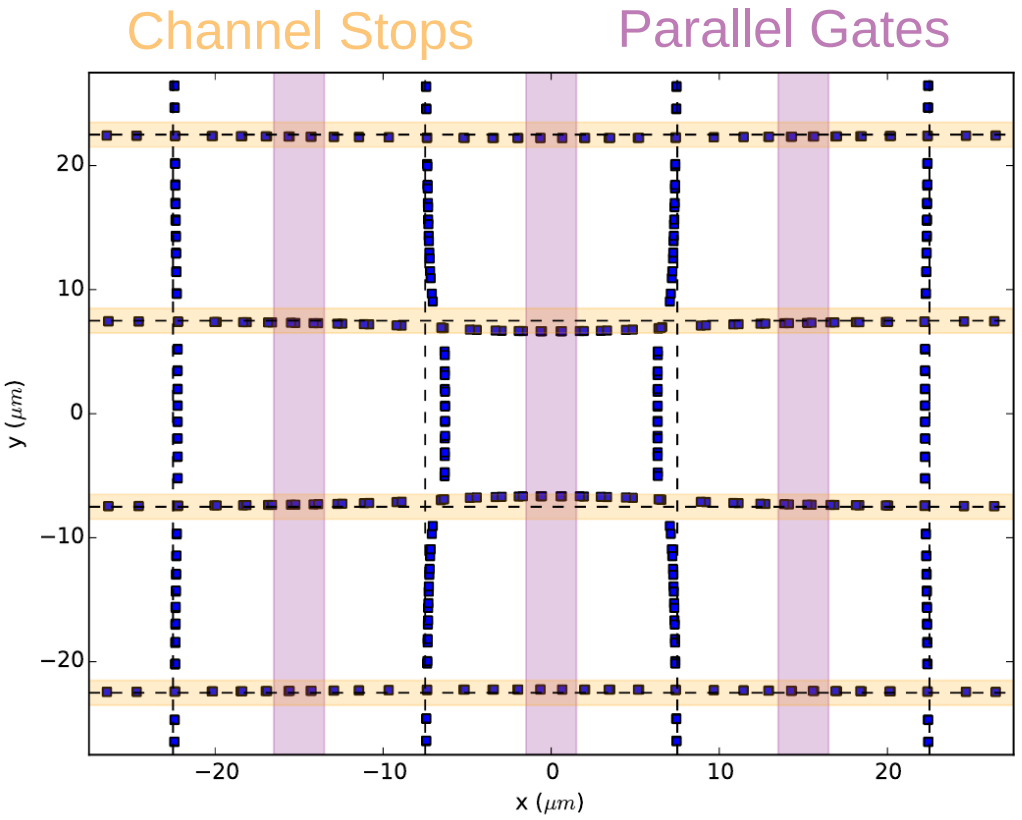


Charge is transferred down columns, then along rows to readout.
Confinement is by gates down columns, and channel stop implants along rows.
LSST pixels are small in area, but very deep (10 micron square, 100 micron deep)

Brighter – Fatter Effect

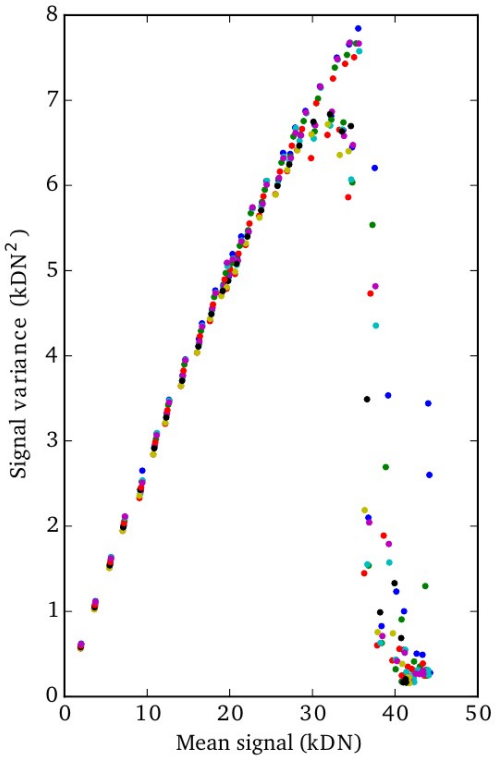


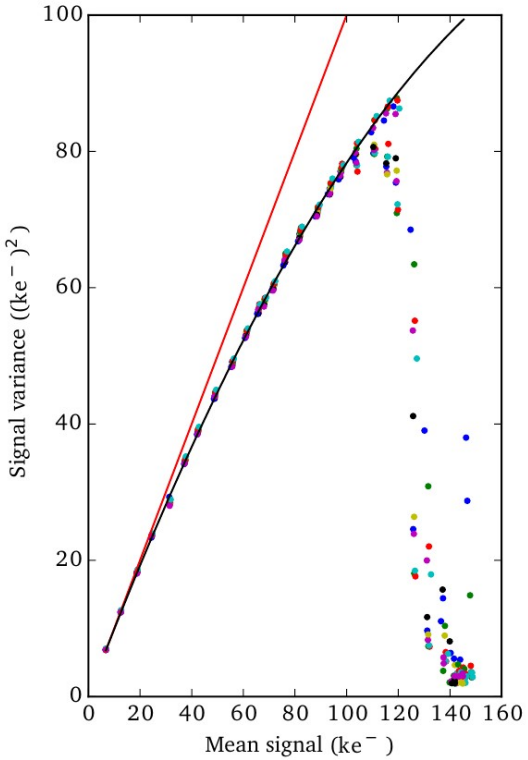
- Charge stored in buried channel causes drift field lines in CCD to change during integration, in effect dynamically moving pixel boundaries
- Left – electrostatic simulation of 75ke point charge stored in CCD (red lines) and empty (black lines)
- Right – simulation of pixel boundary movement with 75ke in central pixel

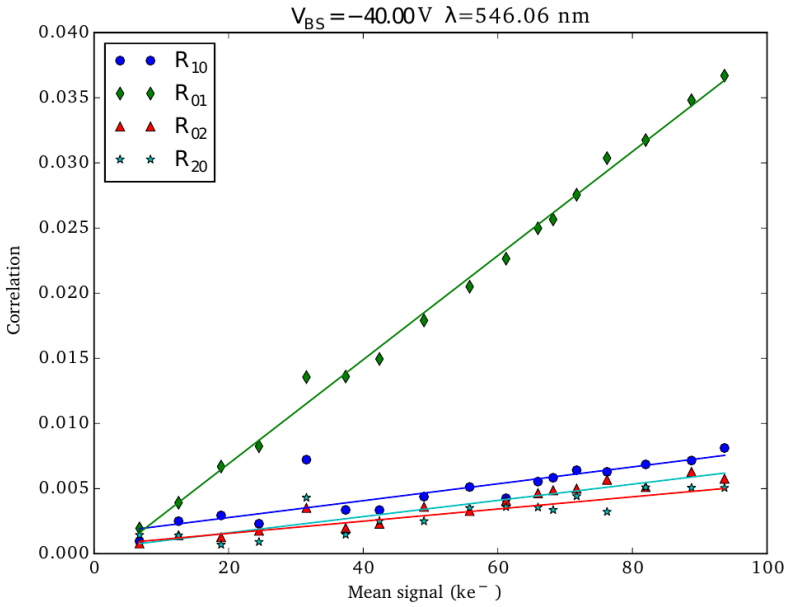


- Note boundary moves more in direction defined by gates than that defined by channel stops in most circumstances – hence the term “brighter-fatter”
- We are aiding the modelling and correction effort for the brighter-fatter effect within LSST using simulations and laboratory measurements.

Gain and Full Well - CCD250



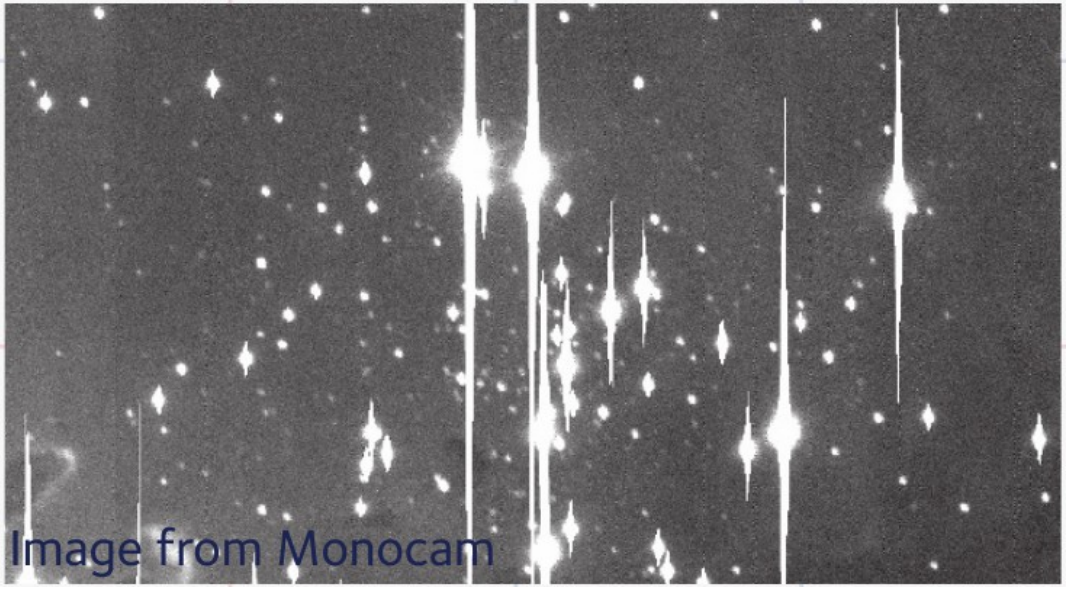


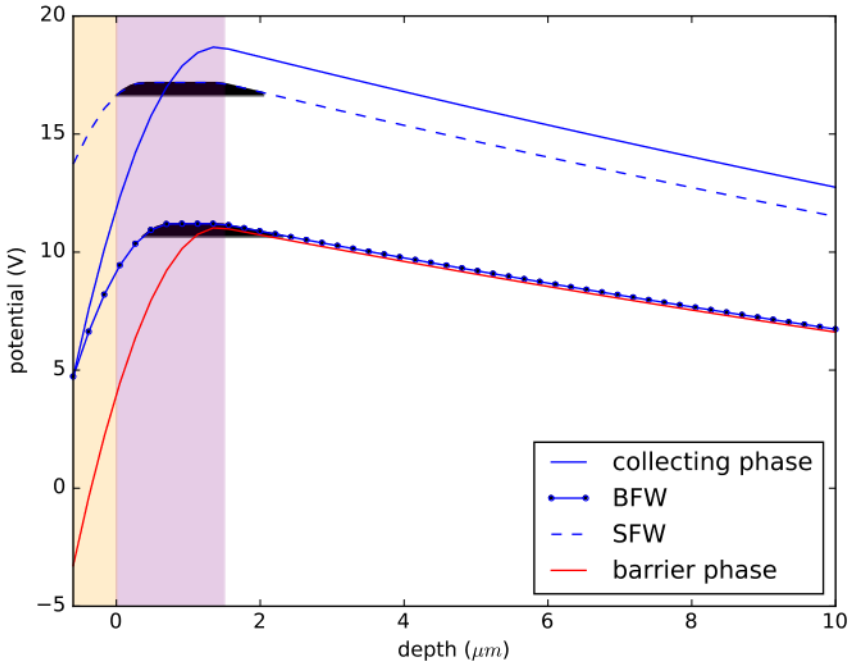


- Gain and full well measured from photon transfer method (above)
- Gain important in terms of other requirements – “full well” specified in electrons, (175 ke max), but “real” requirement is <4V output swing
- Note maximum possible output not the same thing as what we think of as “full well”
- LSST has no official specification / requirement for full well
- Brighter-fatter effect causes mean-variance curve to “roll off” due to correlations

Full Well

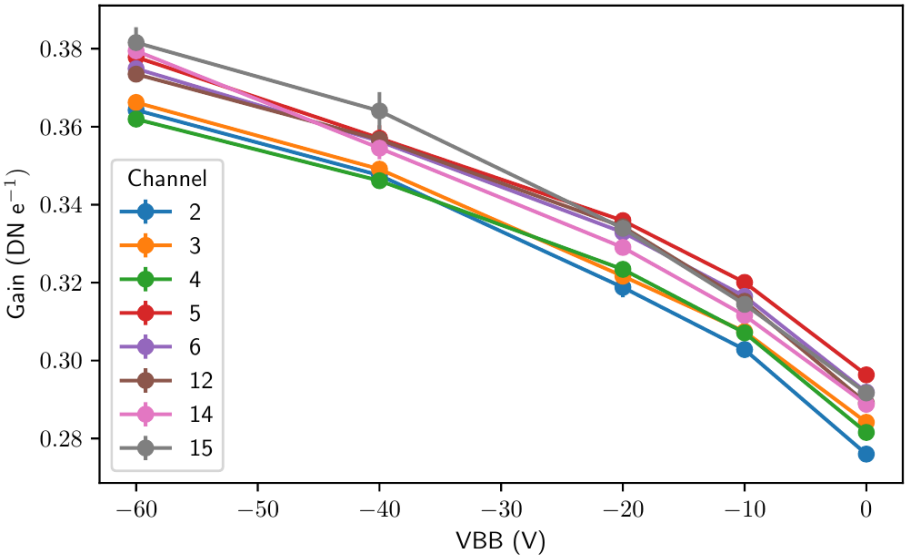
- When full well occurs, over-exposed sources “bleed” up and down the columns (BFW)
- Depending on gate voltage, the electron packet may contact the oxide surface (SFW) before or after this happens
- Maximum full well occurs where these points are equal
- **CCDs should not be operated in SFW condition – it causes many problems with noise, trapping and persistence**





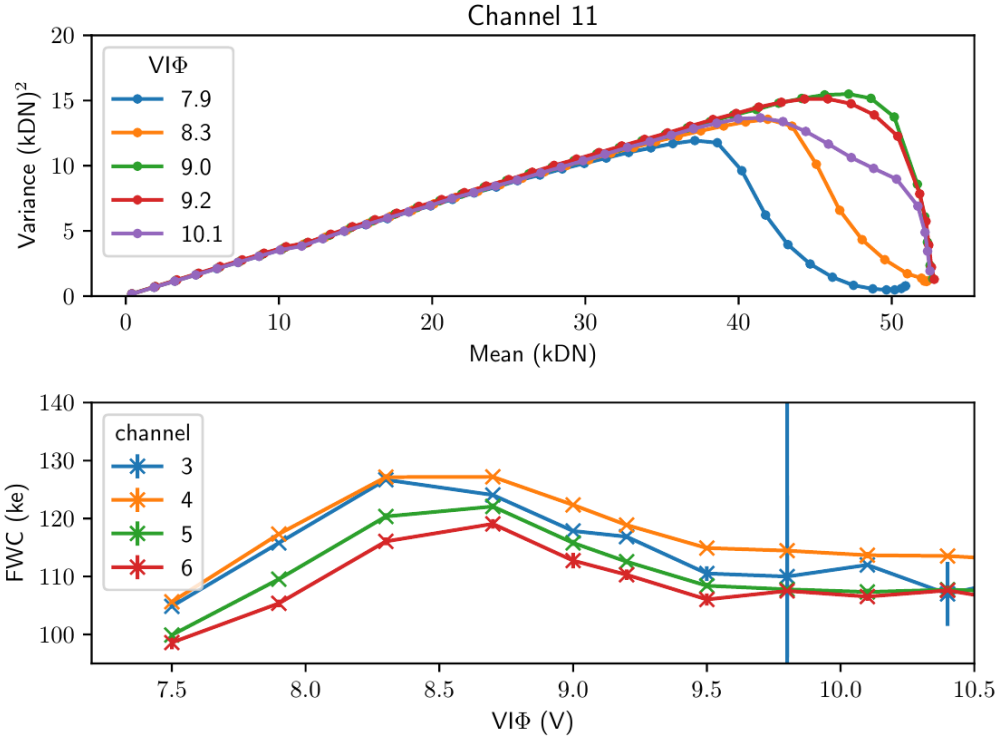
- Full well is highly dependent on material properties and appears to be amongst the most variable parameters
- A slight worry for brighter-fatter effect,
- as bleed trails represent a large amount of charge which will cause distortions nearby.

Voltage Optimisation



Gain (and full well) vary with backside bias (because sense node capacitance changes)
Seen before in other back biased sensors (Robbins 2012), but this variation (~30%) appears larger than any other sensor yet measured

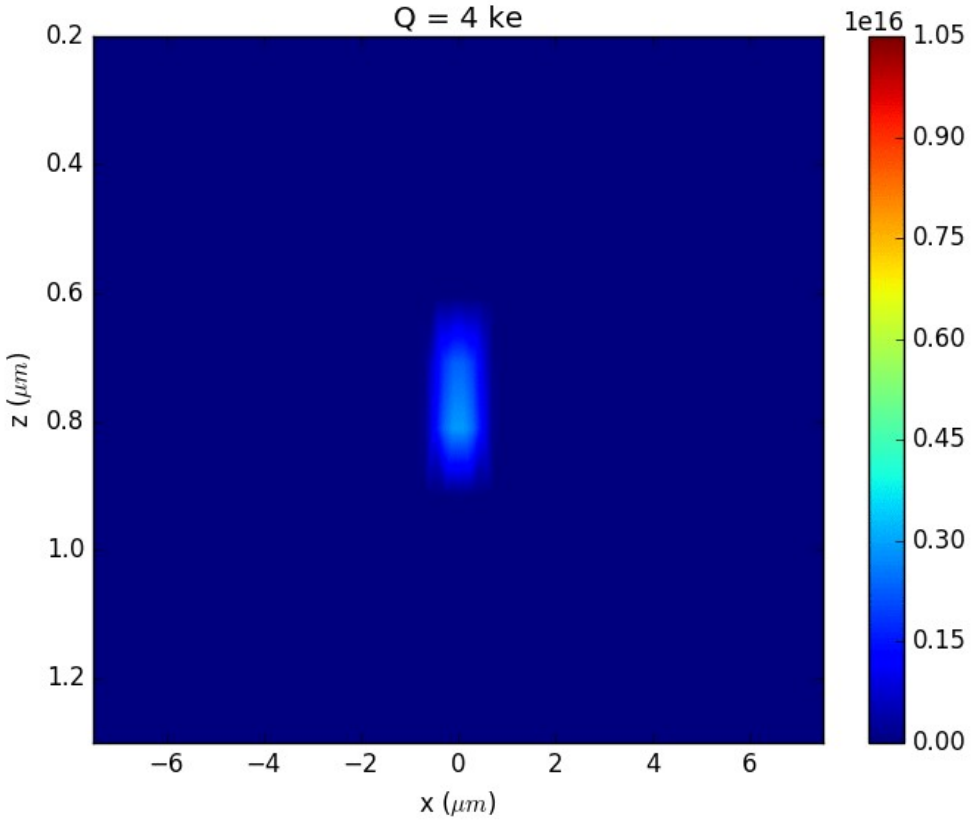
As with all other CCDs, effective full well and surface transport threshold varies with image clocking voltage. We find that the optimum full well point is significantly below the recommended operating point many LSST sensors are (possibly) being operated in the surface transport regime – more investigations needed!



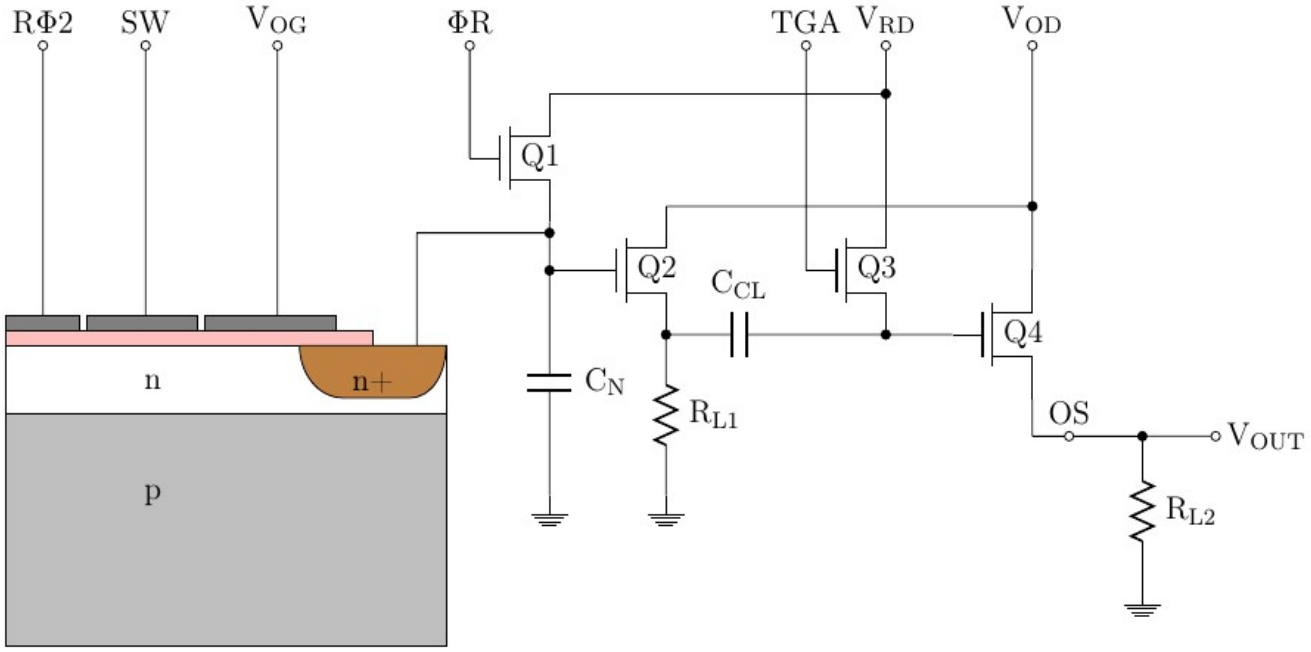
Charge Storage: TCAD modelling

Using commercial TCAD (Sentaurus) software we have assisted in modelling the behaviour of stored charge at high signal levels

Blooming and surface contact effects both clear – junction depth = 1 μm,
Oxide interface @ z=0.2 μm



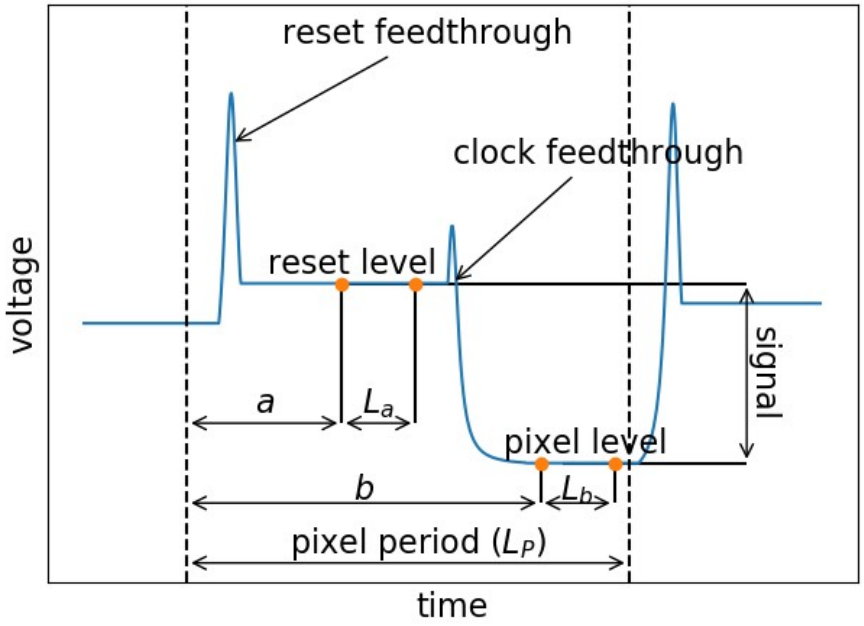
Reset noise & CDS



- Finite bandwidth of the reset transistor causes reset level to fluctuate between pixels.
- If not removed by Correlated Double Sampling (CDS) processing, this reset noise would be the largest component of noise present in CCD readout.
- For T=178 K (LSST nominal) and node capacitance C_N=15fF (typical high responsivity CCD), equivalent of roughly 40 e-.

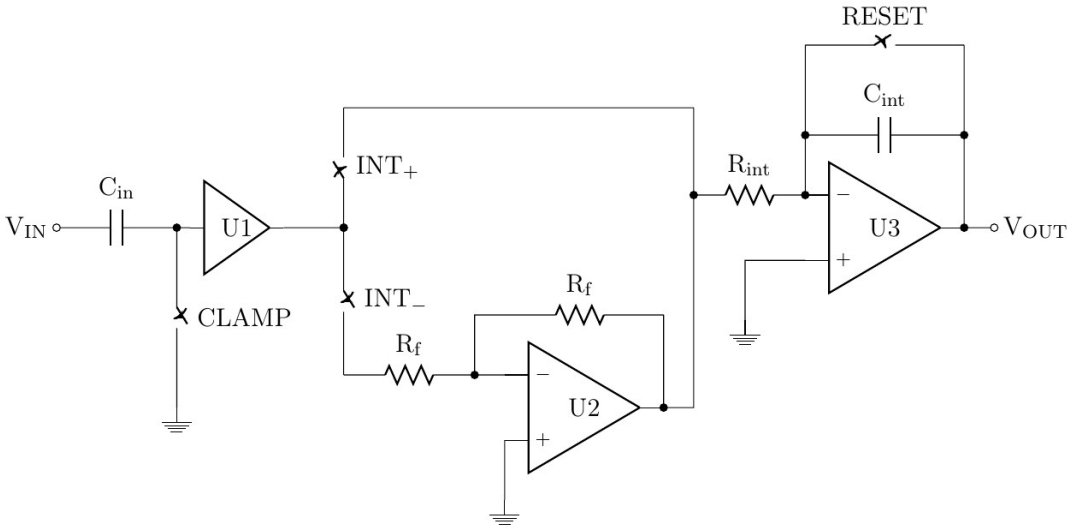
$$N_{\mathrm{rms}} = \sqrt{\frac{k_B T}{C_N}}$$

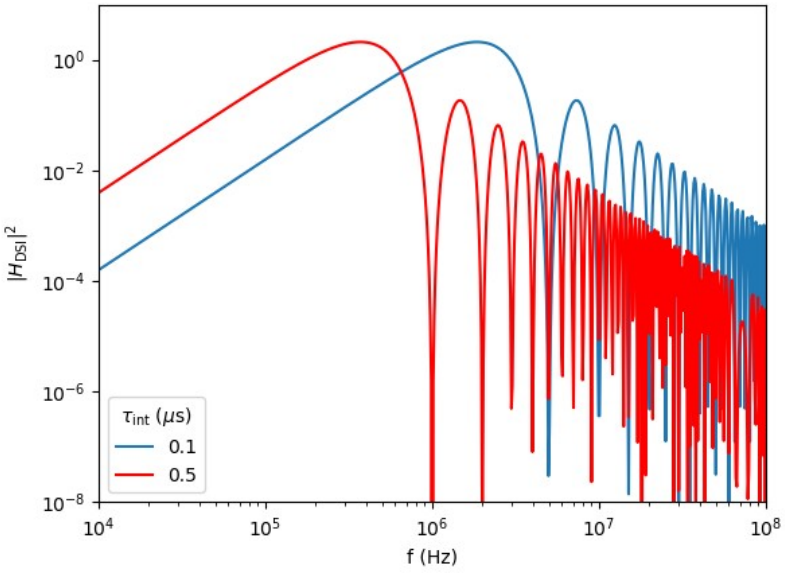
Cancelling reset noise (CDS)



- Integrate over the reset signal, integrate over the pixel signal, and subtract
- Cancels correlated noise (and some broadband noise
- Filter is linear, time invariant, but in practice, **timing is crucial**

$$|H_{\mathrm{DSI}}(f)|^2 = \frac{4\sin^4(\pi f \tau_{\mathrm{int}})}{(\pi f \tau_{\mathrm{int}})^2}$$





STA Archon Controller

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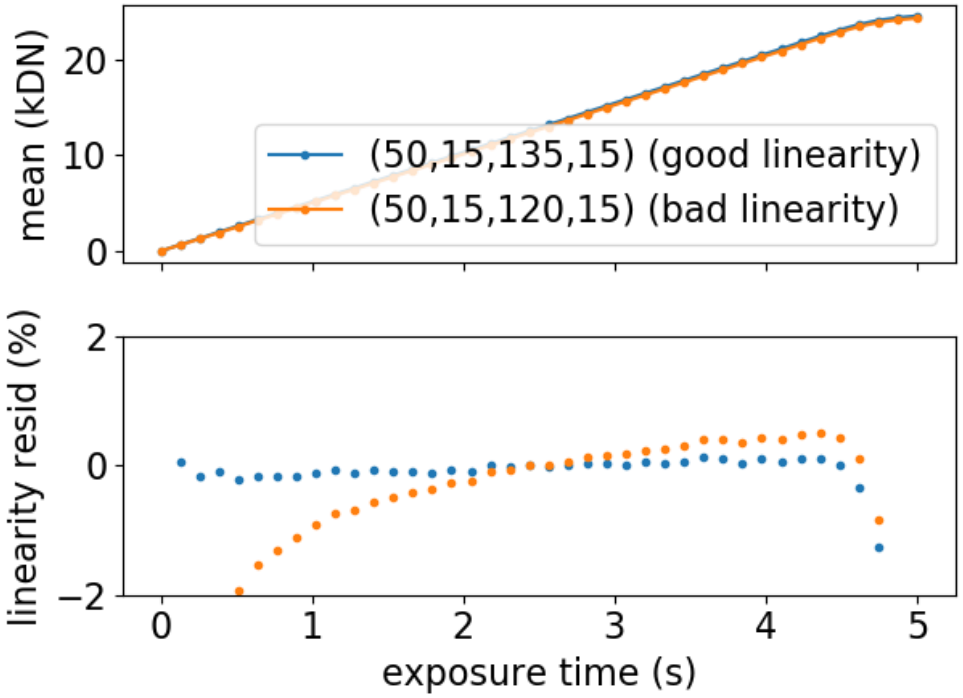
Digital CDS - Perform the same integration via summing highly oversampled signal captured by a fast ADC.

This allows us to adjust CDS timings and see the effects using the <u>exact</u> same physical output data (unavailable in final LSST electronics)

- ADCs operate at 100MHz
- Ability to capture raw data from one channel at a time
- “simple” digital CDS – cannot apply weighting coefficients to each sample
- 4V ADC acceptance range

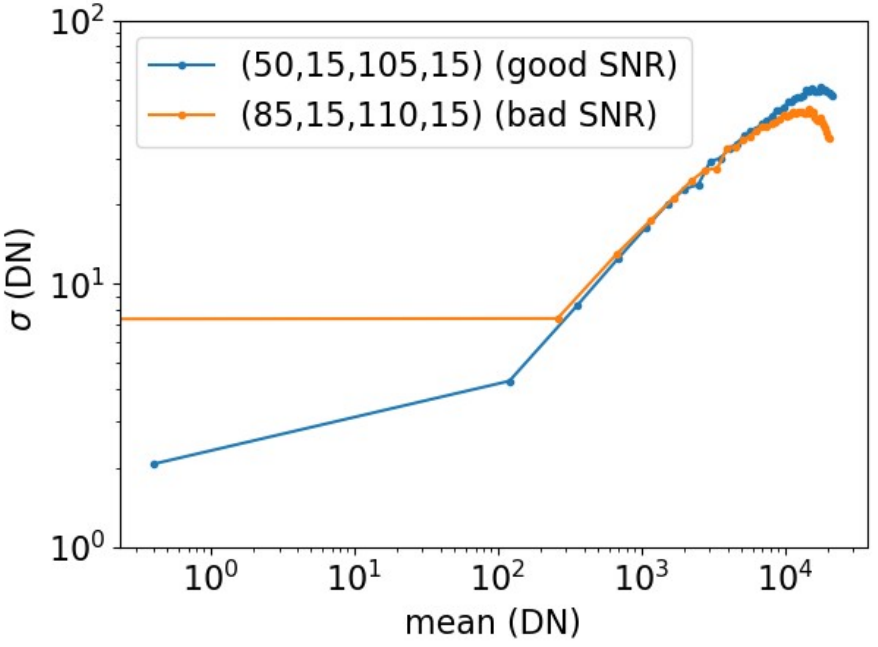
- Archon generates all clock signals, all bias voltages, and handles readout of (in our configuration) up to 16 channels.

Effect of CDS timing on PTC



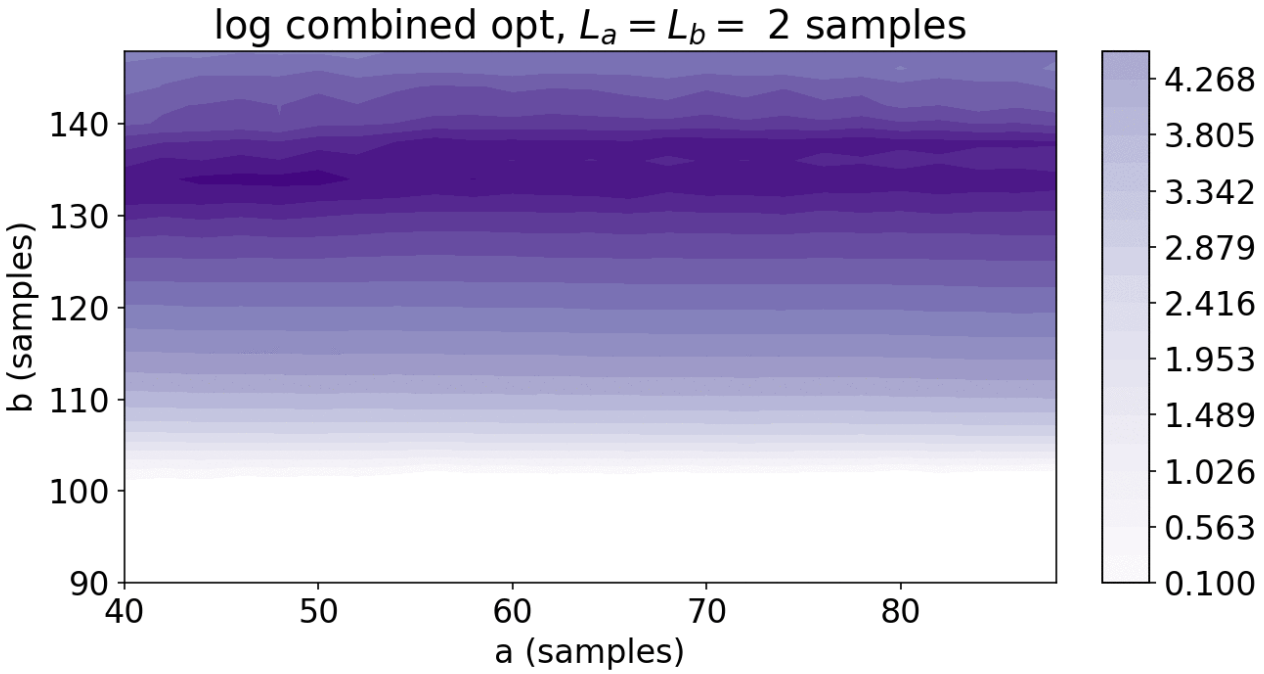
$$\mathrm{LR} = 100 \times \left(1 - \frac{S_{\mathrm{mid}} t}{S t_{\mathrm{mid}}}\right)$$

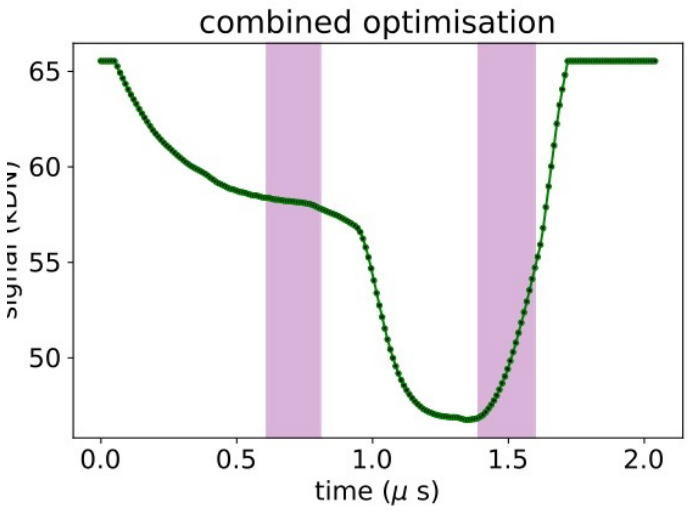
- Residuals calculated in manner following Janesick, 2001.



- Changing CDS timings can affect both linearity and SNR
- Clearly the same set of parameters do not optimise both linearity and SNR.

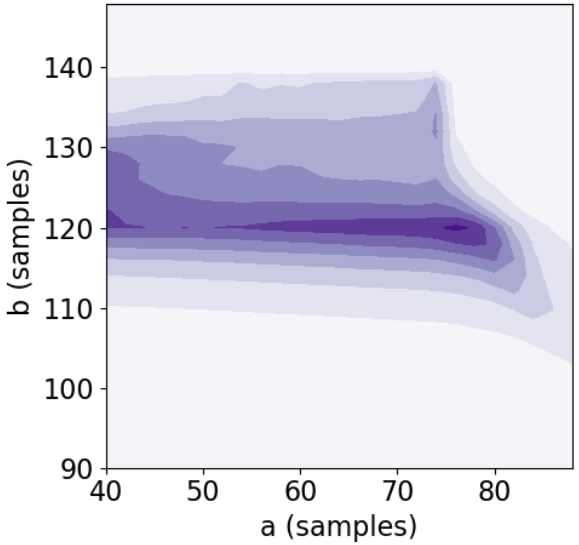
Combined Optimisation

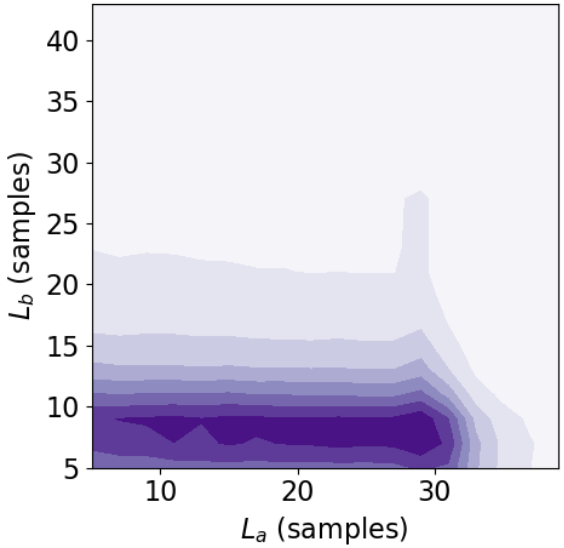




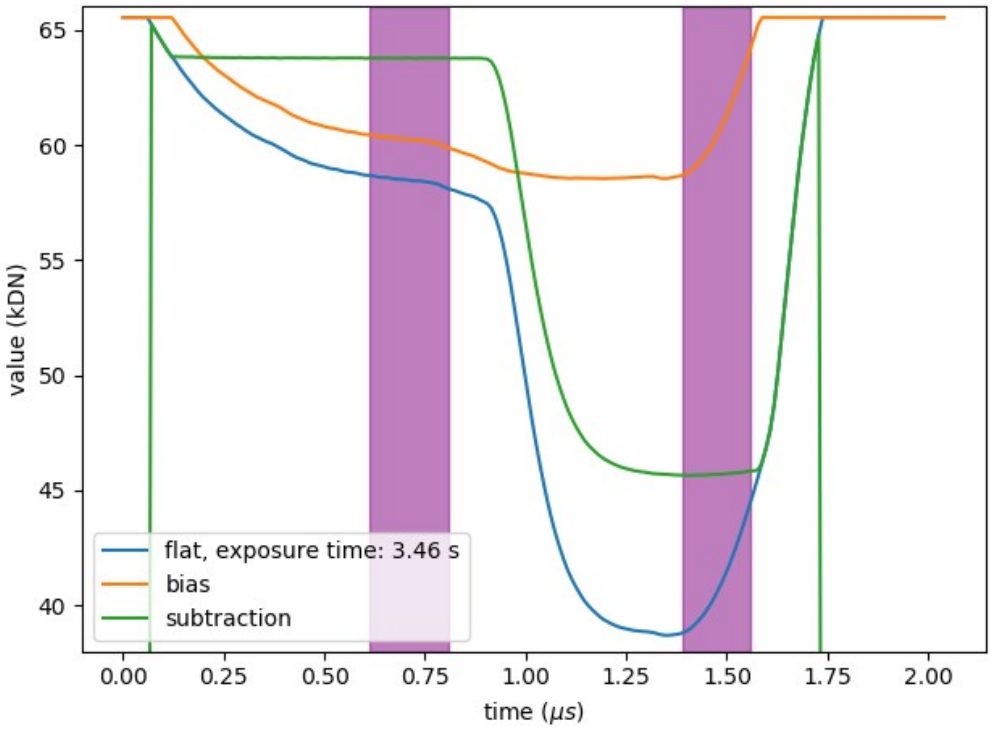
$$f_{\mathrm{cd}} = \frac{f_{\mathrm{SNR}}}{f_{\mathrm{lin}}}$$

- (higher is better)
- Could combine with different powers to emphasize SNR over linearity or vice versa



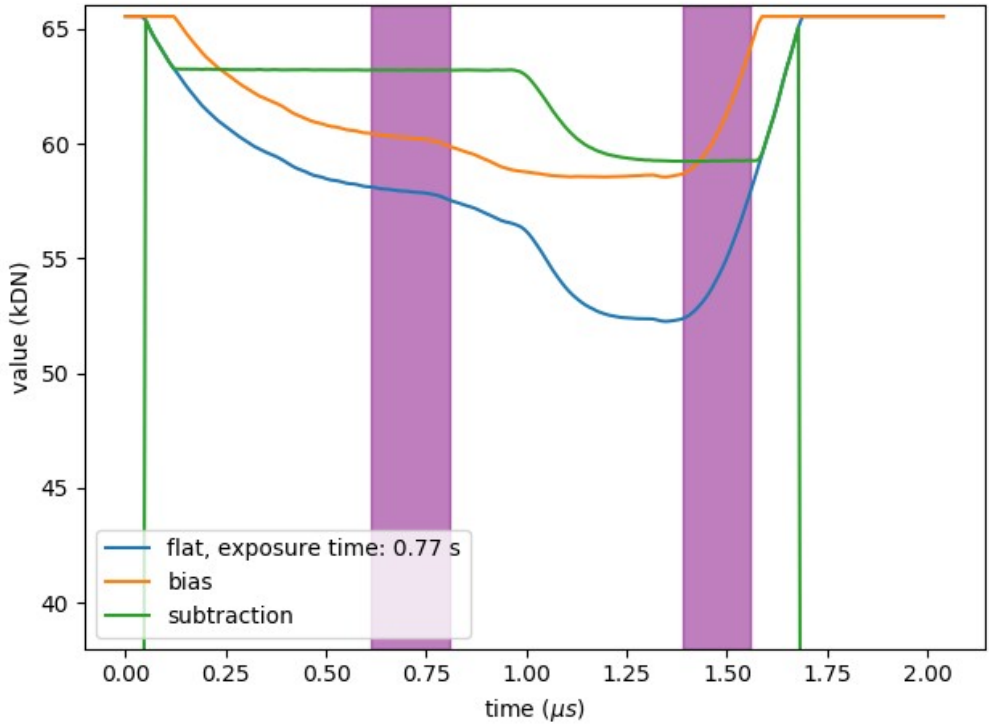


Pixel subtraction

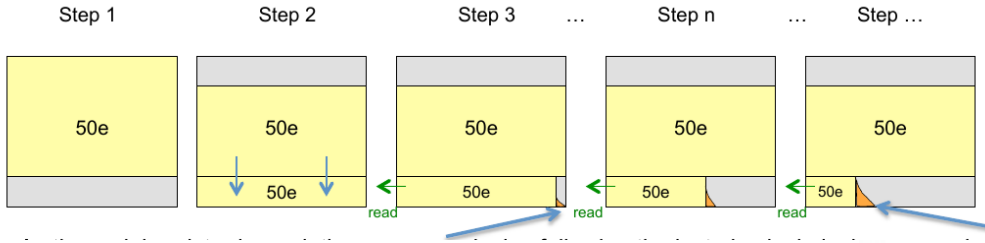


Subtracting the raw samples first allows us to see the origin of the unintuive “late” CDS period which optimises for linearity

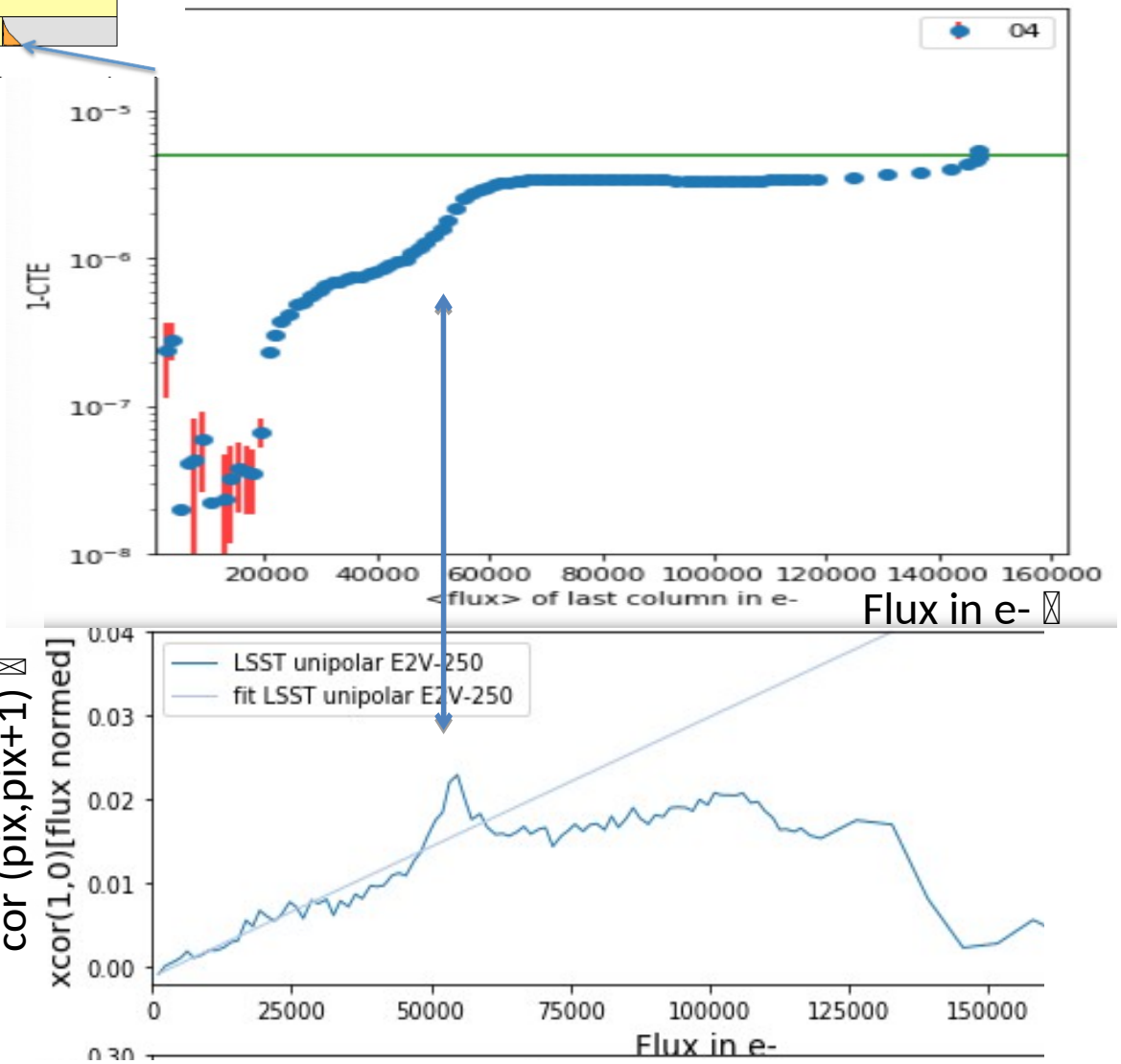
- Note the green lines, which are (flat – bias) subtracted raw sample by raw sample, uncover the more stable nature of the early reset level, and the longer stable region of the signal period
- Could use this to extend method to analog CDS systems via scope captures



Charge Transfer Inefficiency

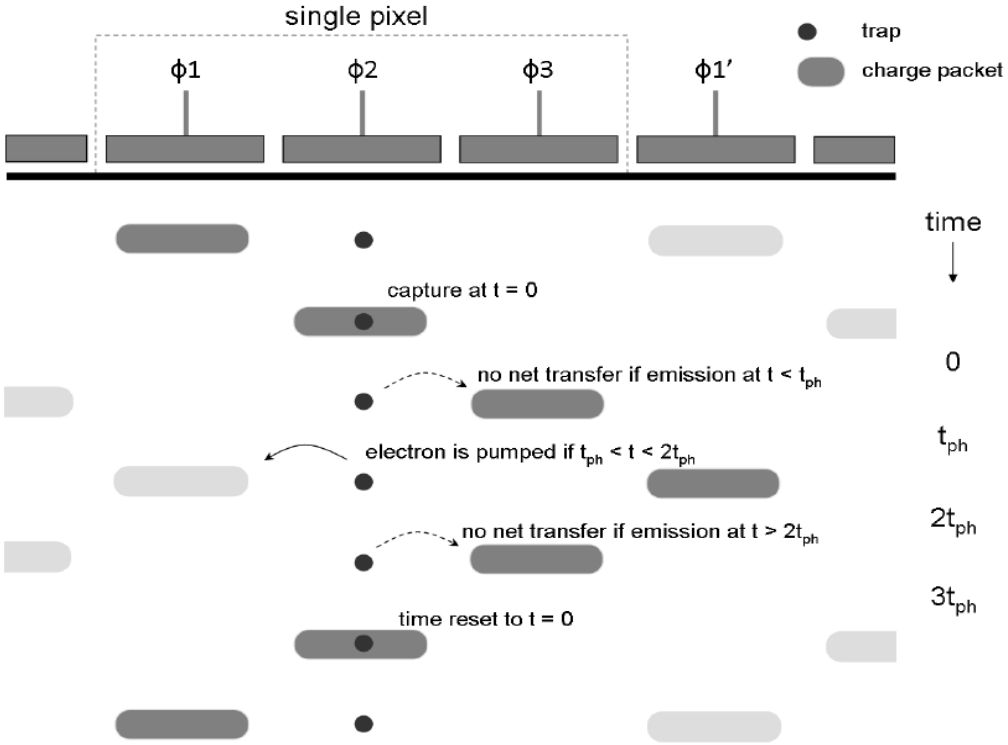


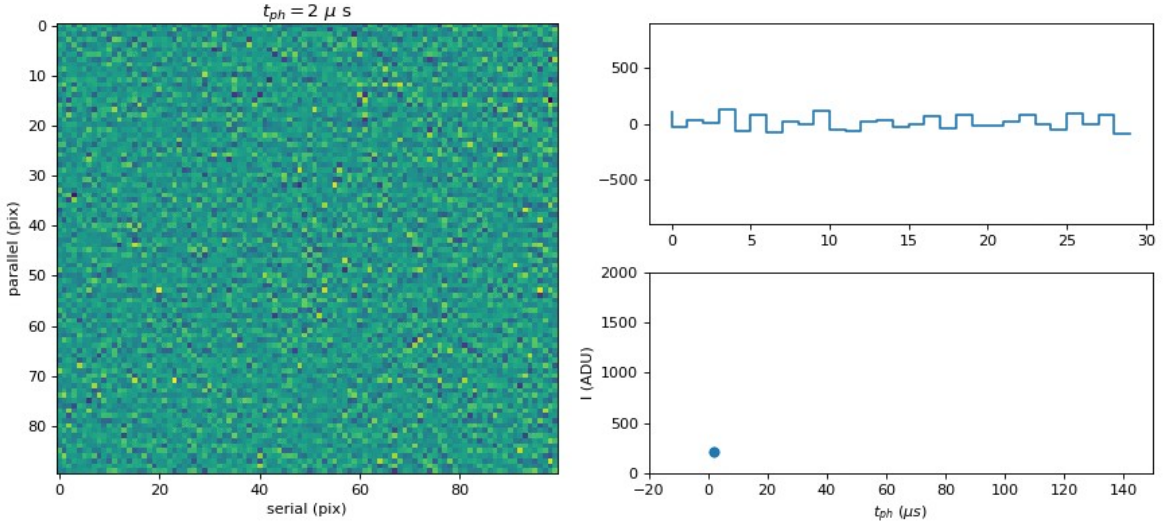
- Charge Transfer Inefficiency (CTI) is a potential problem with the LSST camera – similar size to BFE
- Need to either solve or correct for (spec is CTI < 5E-6).
- In LSST, the **variation of CTI with signal level** will also matter
- Data from Pierre Antilogous (right) shows that CTI variation with temperature also directly injects (none-BFE related) correlations.
- **Not currently included in models of LSST sensor performance**
- We are aiding this investigation through a trap pumping study



Trap Pumping Concept

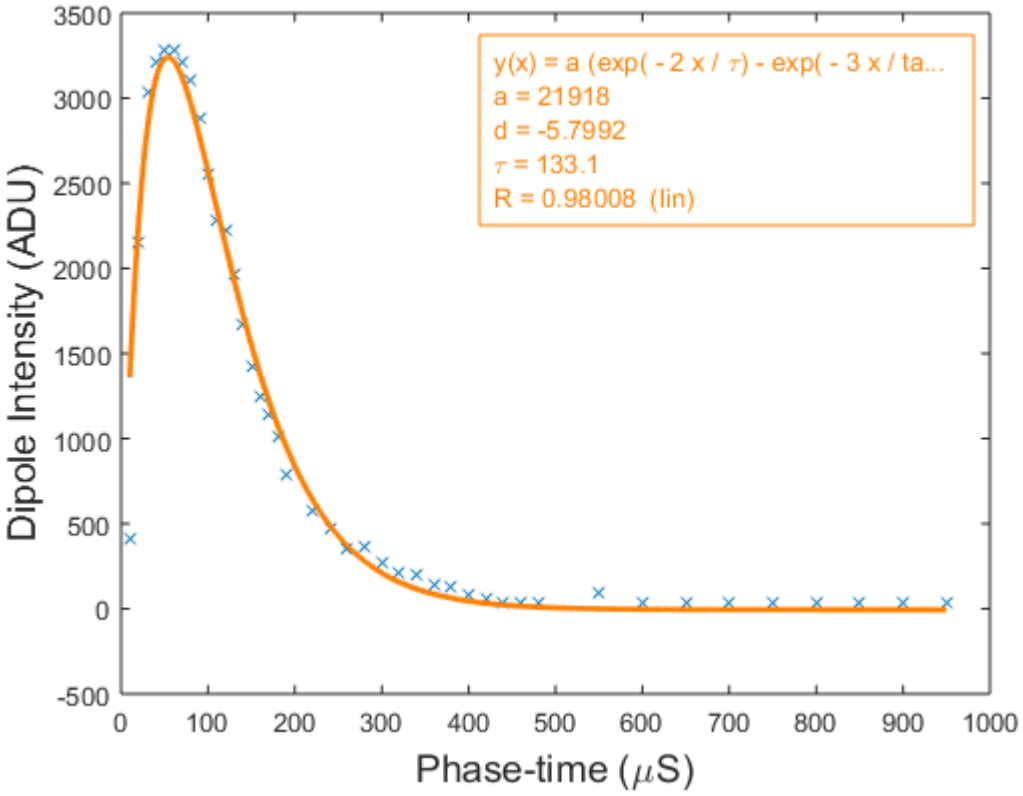
- CTI partly caused by silicon defects (“traps”), but there are other sources too.
- After flat field illumination, repeatedly shuffle charge back and forth under a pixel at a constant rate
- Sometimes, a shallow trapping level will capture an electron from the charge packet.
- Given correct timing, it may release the electron into a neighbouring charge packet
- Illustrated right (from Hall, 2014) for a three-phase
- Signature appears in images (below), by varying phase time and temperature can extract information about trap species present in device





- Emission time & capture probability depend on
  - Temperature
  - Trap cross section
  - Local electron density

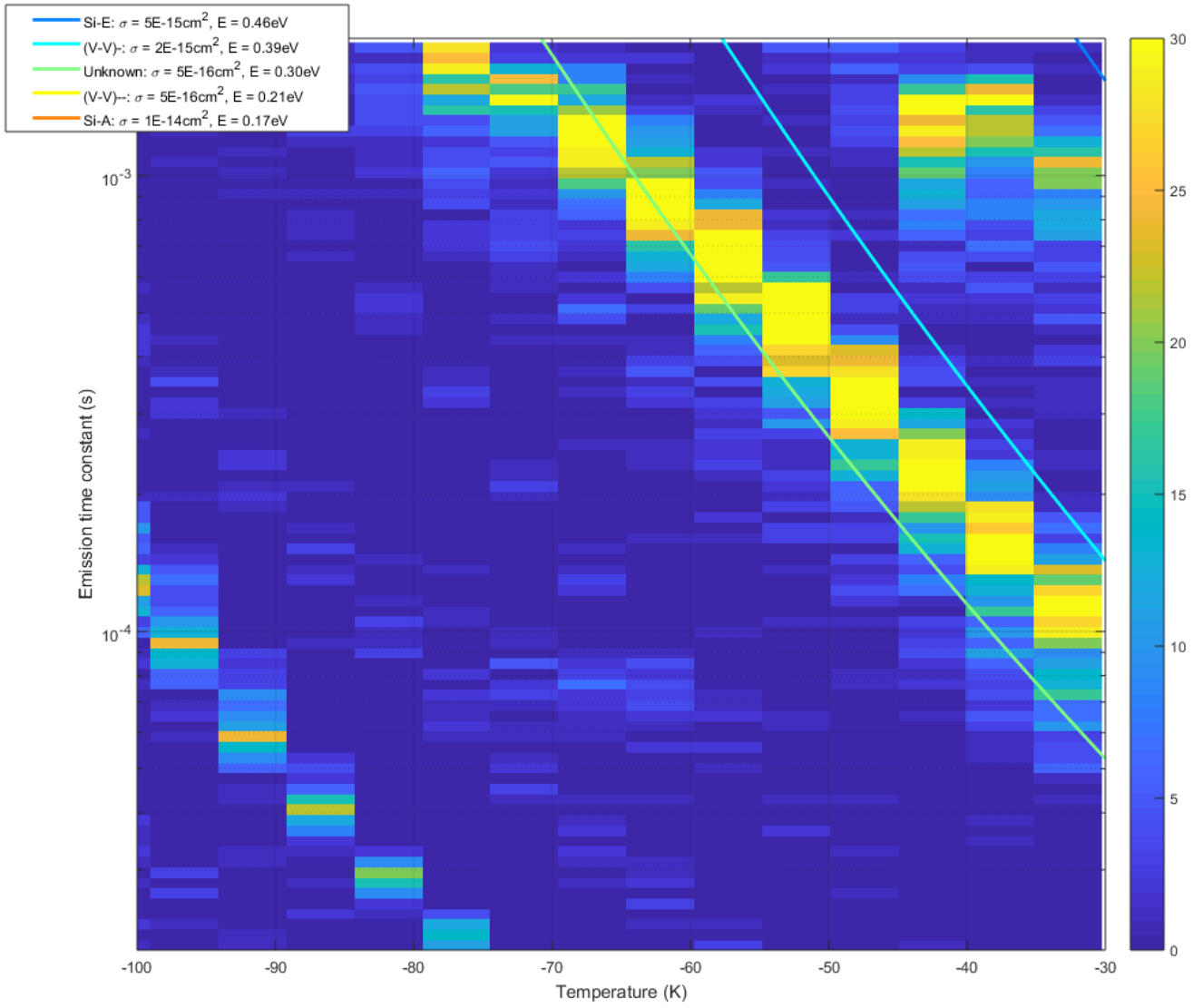
Finding and fitting traps



$$I = N_{\text{pump}} P_c \left(\exp\left(\frac{-2t_{\text{ph}}}{\tau_e} \right) - \exp\left(\frac{-3t_{\text{ph}}}{\tau_e} \right) \right)$$

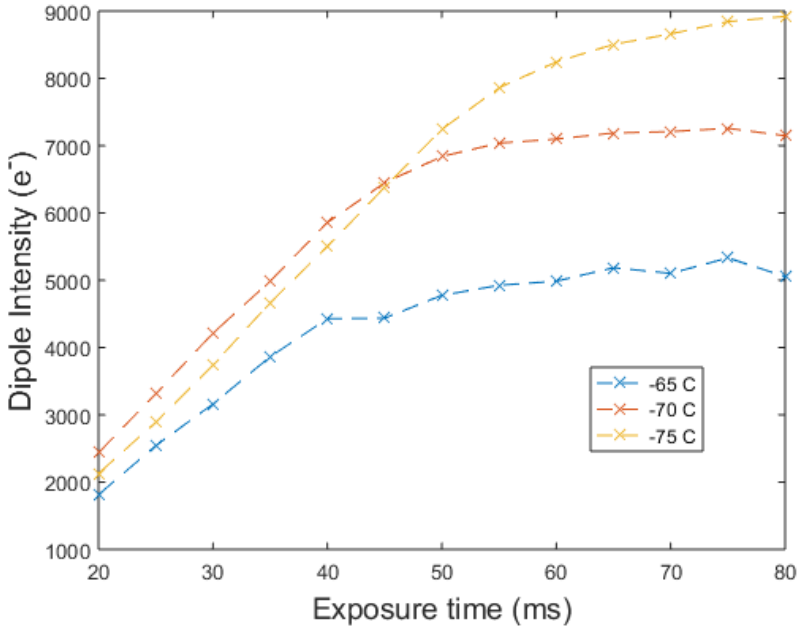
- Procedure: expose to light, then pump a large number of times (50000), varying dwell time. We also take unpumped flats for reference.
- Find traps by simple sigma thresholding (with a goodness of fit cut after fitting emission time curve).
- We typically can get away with 4 sigma exclusion.
- In an unirradiated device, traps are rare!
- Fitting emission time works well for short (above left) and reasonably long (below left) times.
- So far we have taken runs at 5 temperatures, dwell times varying from 20 microseconds to 1000 microseconds.
- Only a few thousand well characterised traps so far

Trap Landscape & timing

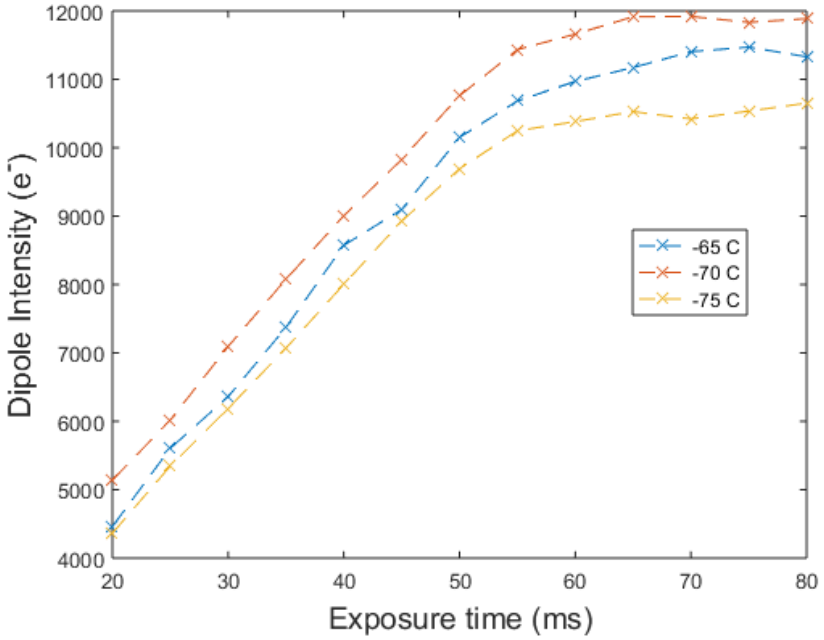


We can from this analysis predict which timing sequences are most “safe” for charge transfer (i.e. avoiding trap emission).
No reason to suspect trap species different in serial & parallel directions, so parallel analysis can inform serial timing choices as well
Experiments still ongoing, initial data shown here from one device (~2000 traps).
Incidentally, we think the largest temperature range trap study ever done, and also the first ever done on a high resistivity device

Trap "Efficiency"



Note the temperature behaviour of efficiency curves can be unexpected – this is because several different temperature varying prefactors involved.



Note maximum possible probability of emission :

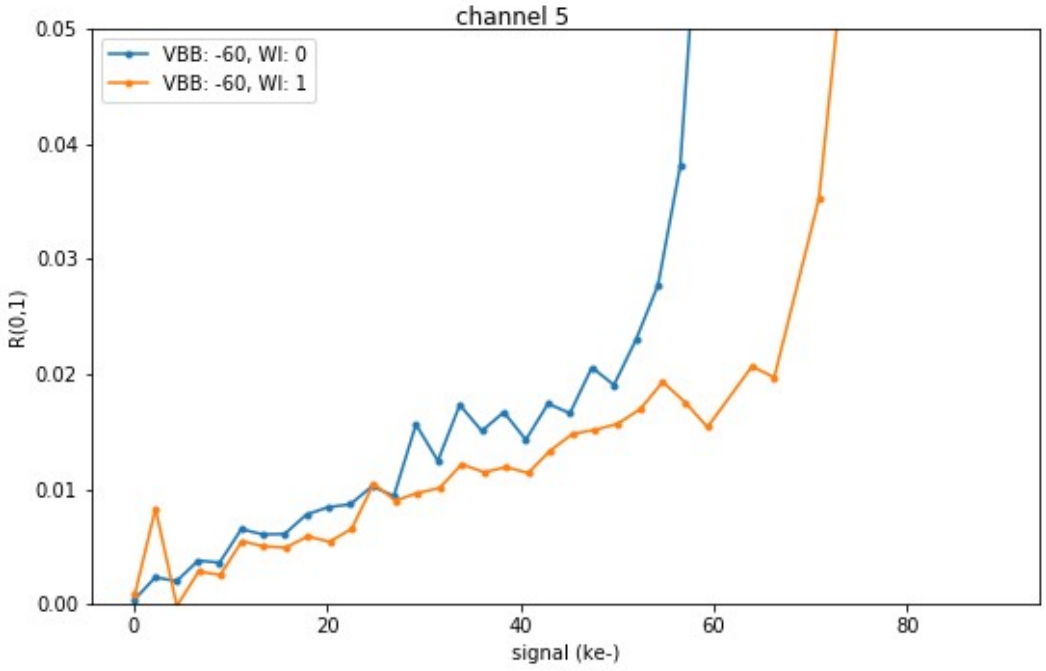
$$\ln\left(\frac{3}{2}\right) = \exp\left(\frac{t_{\rm ph}}{\tau_e}\right)$$

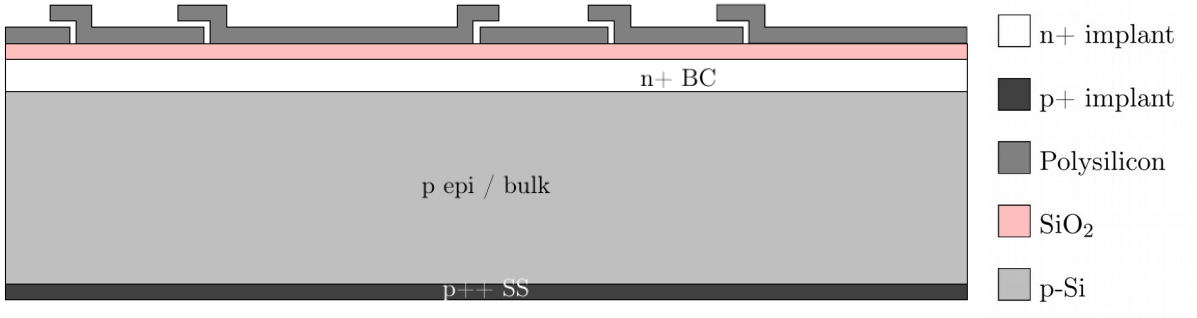
$$P_e^{\rm max} = \left(\frac{2}{3}\right)^2 - \left(\frac{2}{3}\right)^3 \approx 0.148$$

- **Also a possible handle into local charge density measurement – very interesting for the BFE!**

- With N=50000, maximum dipole intensity (for single trap electron) is therefore ~14800e- (i.e. this trap is ~81% capture efficient)
- Variation of trap efficiency **most likely cause** of CTI variation with signal (in our opinion, others think differently!)

Brighter-Fatter gate width





- Change “gate width” by integrating under different numbers of phases
- **Very** preliminnary at this stage, but initial results show this is a larger effect even than back bias voltage.
- Adjusting this comes “for free” in terms of readout time, we are very keen on thoroughly investigating this. It may reduce the needed size of brighter-fatter corrections by ~20%

Thanks for your attention

Daniel.weatherill@physics.ox.ac.uk

With many thanks to:
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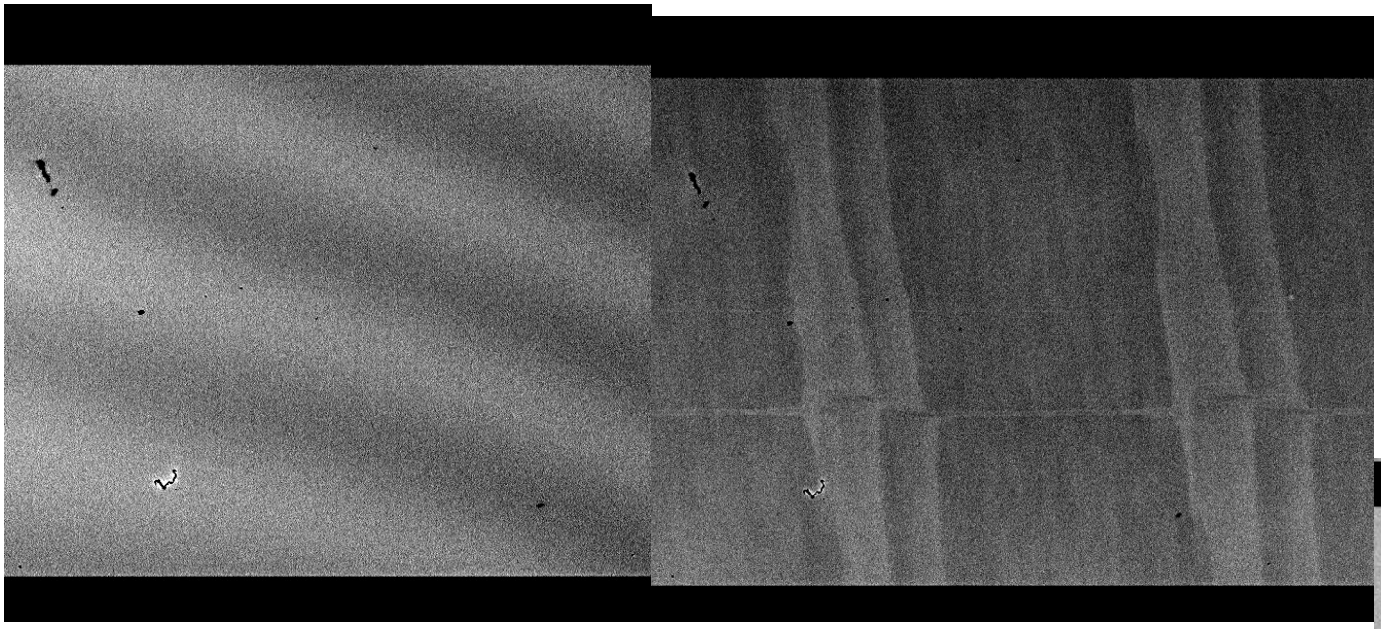
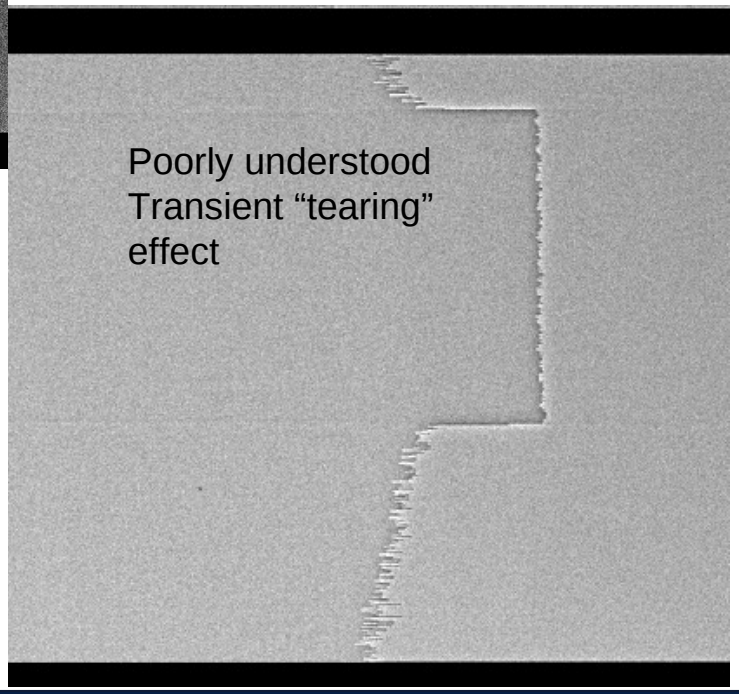
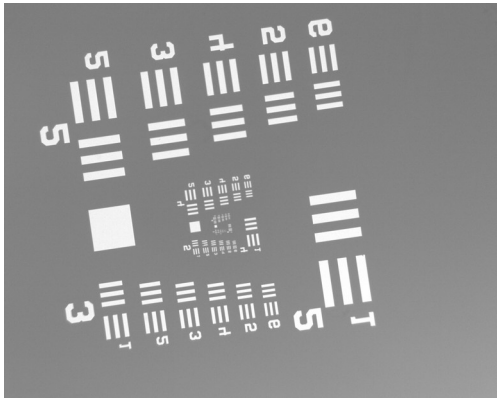
& all other OPMD team members.



Fringing pattern @960nm

Stitching pattern @450nm





Some papers so far:

- Weatherill et al (2017), JINST
- Weatherill et al (2018), JINST
- Weatherill et al (2019), in review for JATIS